measurements at 10°C intervals over the circuit's operating-temperature range.

To compensate for IC_1's temperature variation, you can select from among several possible resistor-thermistor-network topologies. First, you need to select a suitable thermistor and characterize its resistance-versus-temperature variation. Because the MAX1714's current-limit input pin feeds a relatively high input-impedance voltage-follower stage, this thermistor requires a high nominal resistance of 100 kΩ. Resistance-versus-temperature characteristics of inexpensive thermistors exhibit considerable nonlinearity, but one relatively simple approach to linearization involves paralleling the thermistor with a fixed resistor equal to the thermistor's nominal resistance (**Reference 1**). In the network of **Figure 1**, R_1 linearizes the thermistor, and R_2 and R_3, respectively, set the slope and intercept of the current-limit-voltage-versus-temperature-characteristic curve.

To arrive at optimal values for R_2 and R_3, we prepared a spreadsheet incorporating the original current-limit-voltage-versus-temperature data and added columns for each of the network's resistors, plus the thermistor specification sheet's resistance-versus-temperature data. While observing the circuit's temperature-versus-voltage transfer function, we varied the spreadsheet's values for R_2 and R_3 until the transfer function best approximated the measured current-limit-voltage-versus-temperature data. Finally, we constructed the circuit and tested it over the temperature range and noted that it yielded a reasonably flat response.

The curvature of the corrected output characteristic of **Figure 2** (red trace) is intrinsic to the thermistor. Though not perfectly flat, the corrected curve represents a great improvement over the original (black trace) and is sufficient to meet the original design goal. You can achieve more precise compensation by selecting a different thermistor or by incorporating multiple thermistors. **EDN**

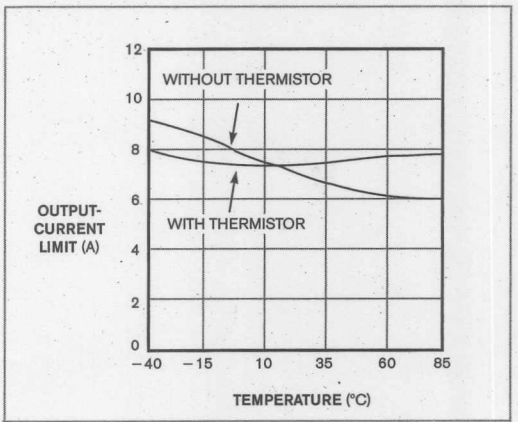

Figure 2 Before (black trace) and after (red trace) current-limit-versus-temperature characteristics show the performance enhancement that the circuit in Figure 1 provides.

REFERENCE

1 Horowitz, Paul and Winfield Hill, *The Art of Electronics*, ISBN 0 521 37095 7, Cambridge University Press, New York, 1980.

Add a Schmitt-trigger function to CPLDs, FPGAs, and applications

Stephan Roche, Santa Rosa, CA

Thanks to its internal hysteresis, the highly useful Schmitt-trigger circuit accepts a low-slew-rate input signal and produces a clean, glitch-free output transition. Unfortunately, user-programmable logic devices, such as CPLDs and FPGAs, generally offer no direct method of synthesizing Schmitt-trigger gates and buffers. This Design Idea shows how a few external components and some VHDL code can implement a Schmitt trigger and put it to work in several useful applications.

To create an equivalent of the basic Schmitt-trigger buffer, you use two external resistors to create positive feedback around a buffer (**Figure 1a** and **b**). You can also use four external resistors to set two threshold levels around an R-S flip-flop (**Figure 1c**). The following equations, respectively, describe the basic Schmitt trigger's positive- and negative-threshold levels:

$$V_+ = \frac{R_1}{R_2} V_{CC} + V_{TH}\left(1 - \frac{R_1}{R_2}\right);$$

$$V_- = V_{TH}\left(1 - \frac{R_1}{R_2}\right).$$

In these **equations**, V_{TH} represents the input-voltage threshold of the CPLD/FPGA device, and V_{CC} is its power-supply voltage.

Based on the equivalent Schmitt-trigger circuit in **Figure 1b**, the low-cost resistance-capacitance oscillator in **Figure 2** requires four external passive components. Resistor R and capacitor C set the circuit's oscillation frequency. Note that the resistance values of R_1

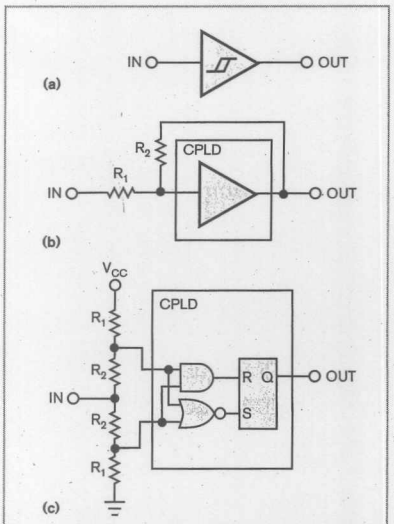

Figure 1 Use a portion of a programmable-logic device or gate array to implement a Schmitt-trigger buffer (a) by adding either two (b) or four external resistors (c).

and R_2 must be larger than that of R. **Listings 1** and **2** contain the circuit's VHDL implementation and RTL architecture, respectively.

In **Figure 3**, an open-collector buffer provides the trigger for the basic Schmitt-trigger-retriggerable monostable circuit by discharging timing capacitor C. The circuit's output pulse width approximately equals the time constant RC. **Listing 3** shows the VHDL implementation and RTL architecture, respectively.

You can convert the retriggerable monostable into the nonretriggerable monostable in **Figure 4** by using an open-collector NAND gate to discharge timing capacitor C. As long as the circuit's output remains high during the timing interval, the system locks out external triggers. As in the previous circuit, the output pulse width approximately equals the time constant RC. **Listing 4** contains the VHDL and RTL codes.

You can use the basic CPLD buffer-with-feedback circuit to provide hysteresis for a contact-debouncing circuit. In **Figure 5**, resistor R_4 provides contact-cleaning current, and R_3 and C form a low-pass filter to reduce noise that contact bounce generates. Component values vary depending on the application. **EDN**

```
Entity Oscillator is
  Port (
        A : in std_logic;
        B : in std_logic;
        OUT : out std_logic
  );
end Oscillator;



architecture RTL of Oscillator is
begin
  A <= B;
  OUT <= not A;
end RTL;



Entity Monostable is
  Port (
        A : in std_logic;
        B : in std_logic;
        Trigger : in std_logic;
        C : out std_logic;
        OUT : out std_logic
  );
end Monostable;
architecture RTL of Monostable is
begin
  A <= B;
  OUT <= not A;
  C <= '0' when Trigger= '1' else 'Z';
end RTL;



  Port (
        A : in std_logic;
        B : in std_logic;
        Trigger : in std_logic;
        C : out std_logic;

          OUT : out std_logic
    );
 end Monostable;
 architecture RTL of Monostable is
 begin
   A <= B;
   OUT <= not A;
   C <= '0' when Trigger= '1' and A='0' else 'Z';
 end RTL;
```

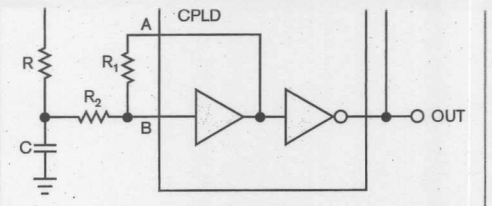

Figure 2 Add a resistor and capacitor to a basic Schmitt-trigger buffer to form a low-cost oscillator.

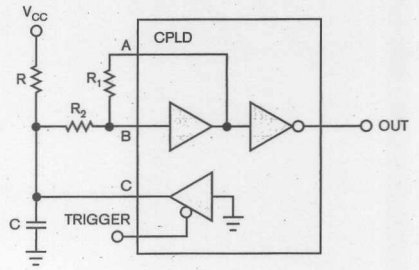

Figure 3 An active-low buffer holds timing capacitor C discharged in this version of a retriggerable monostable multivibrator based on the Schmitt-trigger buffer.

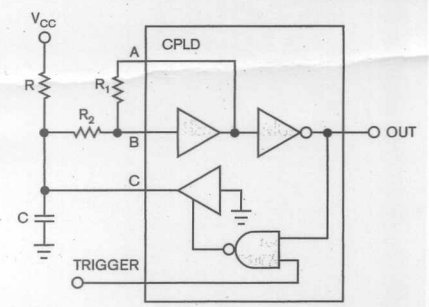

Figure 4 A NAND gate locks out trigger pulses, forming a nonretriggerable, monostable circuit.

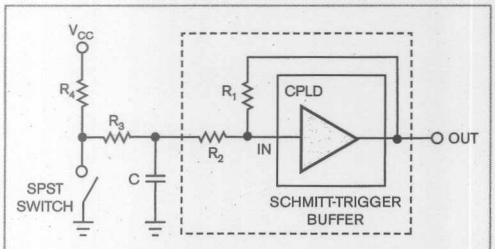

Figure 5 Use a Schmitt trigger to debounce switch contacts.